**Institute of Business and Information Technology**

**Faculty of Business, Economics and Administrative Sciences**

**University of the Punjab, Lahore**

# Course Outline

| Program | BBIT | Course Code | IT-211 | Credit Hours | 3 |
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| **Course Title** | Digital Logic Design | | | | |

## Course Introduction

This course covers the design of integrated circuits for the digital systems. Emphasis is placed on theoretical concepts and systematic techniques of synthesis which can be applied to realistic digital systems design.

## Learning Outcomes

After the completion of this course, it is expected that students who will involve themselves in the knowledge base working of the course will be capable to

1. Design logic level models, including Boolean algebra, Arithmetic Circuits, State Machines and ALU.
2. Design sequential circuits, including latches, flip-flops, registers and counters.
3. Understand the role of time, frequency and interrupts in digital computers.
4. Understand memory, including flip flops, RAM and ROM.
5. Understand and design of control, data and address bus along with their communication with ALU, memory and I/O devices

| | Course Content | Assignments/Readings |
|---|---|---|
| **Week 01** | Digital Systems and Digital Numbers<br>Number Systems and Conversions, Complements | |
| **Week 02** | Boolean Algebra and Circuit Design<br>Basic Logic Gates, Boolean Theorems, Boolean Algebra, Introduction to Verilog HDL | Assignment 1 (a) |
| **Week 03** | Standard and Canonical Forms<br>Standard and Canonical forms; Sum of products and sum of minterms, Product of sums and product of maxterms | Quiz 1 |
| **Week 04** | Gate-level Minimization, MSI Logic Circuits<br>Simplification of Boolean Expressions using K-Map, NAND and NOR implementations, Decoders, Encoders, Data Selectors, Data Distributors | Assignment 1 (b) |
| **Week 05** | Sequential Circuits<br>Sequential Circuits Latches and Flip flops Analysis of clocked sequential circuits | Quiz 2 |
| **Week 06** | Registers<br>Data Storage and Transfer: Registers, Serial Data Transfer: Shift Registers | Assignment 2 (Verilog HDL) |
| **Week 07** | ALU Design<br>Arithmetic Circuits, Analysis and Design procedures of Combinational | Assignment 3 ((a & b) (Design + VHDL) |
| **Week 08** | ALU Design<br>Circuits, ALU integrated Circuits | |
| **Week 09** | **Mid Term Examination** | |
| **Week 10** | Synthesizable HDL Models of Sequential Circuits | |
| **Week 11** | Counters<br>Ripple counters, Parallel Counters, HDL for Registers and Counters | Term Project Proposal |
| **Week 12** | RAM Architecture, RAM Read/Write Operations<br>Random Access Memory (RAM) Architecture, RAM Read/Write Operations | Quiz 3 |
| **Week 13** | ROM Architecture, ROM Operations<br>Memory Decoding, Read-only Memory | Term Project Deliverable 1 |

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| **Week 14** | Register Transfer Level (RTL), RTL in HDL | Assignment 4 |
| **Week 15** | Algorithmic State Machines (ASM)<br>Mealy FSM, Moore FSM | Term Project Deliverable 2 |
| **Week 16** | Synchronizing Data Bus, Control Bus and Address Bus operations with ALU and Memory | Quiz 4<br>Term Project Final Evaluation |
| **Week 17** | Synchronizing Data Bus, Control Bus and Address Bus operations with ALU and Memory | Finalizing Sessional Activities |
| **Week 18** | **Final Term Examination** | |

## Textbooks and Reading Material*

**Textbooks.**

**A.** Digital Design 4th Edition by Morris Mano

**B.** Digital Systems: Principles and Applications by Ronald J. Tocci 10th Edition

**C.** Fundamentals of Digital Logic with VHDL design 3rd Edition by Stephen Brown

## Teaching Learning Strategies

1. The students are expected to have studied the assigned reading, before coming to the class
2. Discussion is generated on key concepts, issues, problems, and solutions on assigned readings
3. Critical discussion on apparent solutions regarding issues pertaining to self, history, knowledge, economy, society, and the state are addressed through questions and arguments

## Assignments: Types and Number with Calendar

1. Session assigned readings for all sessions – evaluation of class participation
2. Presentation, one from each student as part of a group
3. Group assignment – one per student per group
    - It is further divided into five sub assignments, all culminating into final report